

REMARKS

Claims 1-21 are presented for further examination. Claims 1, 2, 7, 14, and 18 have been amended. Claims 20 and 21 are new.

In the Office Action mailed March 27, 2003, the Examiner rejected claims 1-14 and 18 under 35 U.S.C. § 112, second paragraph, as indefinite because of informalities in claims 1, 7, 14, and 18. Applicants have amended these claims to overcome the indefiniteness as identified by the Examiner.

Claims 1, 6-9, and 13 were rejected under 35 U.S.C. § 102(a) as anticipated by the admitted prior art. Claims 10 and 11 were rejected under 35 U.S.C. § 103(a) as unpatentable over the admitted art in view of U.S. Patent No. 6,055,148 ("Grover et al."). Claims 15-17 and 19 were allowed. Claims 2-5, 12, 14, and 18 were found to be allowable if rewritten or amended to overcome the rejections under 35 U.S.C. § 112.

Applicants respectfully disagree with the bases for the rejections and request reconsideration and further examination of the claims.

Applicants have amended the drawings to overcome inadvertent errors. In particular, the legend "N" has been added to the region 32 (described at page 4, lines 5-6) in Figure 2 and the "N" for region 31 has been corrected to read "N⁺" (described at page 4, line 4), and the legend "N⁺" has been removed from portion 5b of the copper plate 5. In Figures 2 and 5, the legend "N⁺" has been added for region 7 (see page 2, line 22). In Figure 5, a line has been drawn on the bottom of region 31, with the portion below the line representing the adhesive layer 108 (see page 8, line 13), and the number "33" on the left has the leader line pointing to the third epitaxial layer and is now amended to read "32." In Figure 5, the upper diode 25 is now referenced with the number "26" and the lower diode is referenced with the number "25."

In the rejection under 35 U.S.C. § 102(a) the Examiner noted that the element 3e in Figure 1 connected between a "common intermediate node 24 and the second high-voltage region 30" corresponded to the recited biasing means. Applicants respectfully disagree and believe there may be confusion between the external diodes 54, 55 of Figure 1 and the integrated diodes 25, 26 of Figure 2. More particularly, in Figure 1 the external diodes 54, 55 are provided (as described at page 5, lines 22-27) as having an intermediate node that *is not* connected to a

second high-voltage region 30. The only possible connection would be through the diodes themselves, particularly diode 54. In Figure 2, the integrated diodes 25, 26 have an intermediate node 24 that is connected through a second annular region 19 and a metallization region 23 to a zener diode 21 that is normally open and in turn connected to a metal gate contact region 22. Thus, in Figure 2 there is no connection between the node 24 and the second high-voltage region 30.

Turning to claim 1, recited therein is an integrated power device that comprises a power component including a first high-voltage region, a low-voltage region, a first unidirectional element and second unidirectional element connected together between the first high-voltage region and the low-voltage region, the first and second unidirectional elements defining a common intermediate node. Claim 1 further recites a biasing means connected between the common intermediate node and a second high-voltage region and configured to connect the intermediate node directly to the second high-voltage region. As discussed above, nowhere is there any teaching or suggestion in Figures 1 and 2 of directly connecting the common intermediate node to a second high-voltage region. Rather, in Figure 1 and in Figure 2 the common intermediate node is not connected to any high-voltage region. Moreover, even if one were motivated to combine the admitted prior art with the teachings of Grover, the resultant device would fall short of the invention as recited in claims 10 and 11.

In view of the foregoing, applicants respectfully submit that claim 1 as well as dependent claims 6-11 and 13 are clearly allowable over the references cited and applied by the Examiner.

New claim 20 is a combination of allowable claim 2 and independent claim 1. New claim 21 is a combination of allowable claim 12, intervening claims 9-11, and independent claim 1. Applicants respectfully submit that claims 20 and 21 are allowable for the reasons why claims 2 and 12 are allowable.

In view of the foregoing, applicants submit that all of the claims in this application are in condition for allowance. In the event the Examiner finds minor informalities that can be resolved by telephone conference, the Examiner is urged to contact applicants' undersigned representative by telephone at (206) 622-4900 in order to expeditiously resolve

Application No. 10/038,753
Reply to Office Action dated March 27, 2003

prosecution of this application. Consequently, early and favorable action allowing these claims and passing this case to issuance is respectfully solicited.

The Commissioner is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

Respectfully submitted,

Romeo Letor et al.

SEED Intellectual Property Law Group PLLC



E. Russell Tarleton

Registration No. 31,800

ERT:aep

Enclosures:

Postcard

Replacement Sheets

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

399948_1.DOC